REMARKS

This is in response to the Office Action dated November 15, 2005. Claims 9-15, 28, 35-37 and 42 are pending.

Claim 9 stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Jung Mok (US 5,923,390). This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 9 requires "a storage capacitor common line disposed parallel to the signal line so as to be electrically connected to the storage capacitor electrode, the storage capacitor common line extending across a plurality of pixels, wherein storage capacitance is provided between the pixel electrode and the storage capacitor electrode, the scanning line and the storage capacitor electrode are fabricated from a same material in a single patterning; and wherein the storage capacitor electrode and the storage capacitor common line are patterned in different steps so as to have an insulating film provided partially therebetween." For example, and without limitation, Fig. 24 of the instant application illustrates storage capacitor common line 14 disposed parallel to signal line 11. This feature is advantageous, for example and without limitation, in that a lower time constant of the signal lines may be realized. In particular, for example and without limitation, the instant specification on page 20, lines 8-16, describes the advantageous effect of realizing a relatively low time constant of the signal lines, which is derived from the electrostatic capacity between the signal lines and the other wires that is reduced by the signal lines crossing none of the storage capacitor common lines in a central area of the device; see also page 73, line 24 to page 74, line 9.

The Fig. 4-6 embodiment of Jung Mok fails to disclose or suggest the aforesaid underlined feature of claim 9. Instead, in the Fig. 4-6 embodiment of Jung Mok, the capacitor

common line/wiring 81b is parallel to the scanning line 60 – *not* to the signal line 70. In other words, in the Fig. 4-6 embodiment of Jung Mok the capacitor common line 81b is *perpendicular* to the signal (source) line 70; not "*parallel*" to it as claim 9 requires. Thus, not only does Jung Mok fail to disclose or suggest the invention of claim 9, but it teaches directly away from the same.

In the Office Action dated November 15, 2005, the Examiner argued that in Figs. 4-6 of Jung Mok ITO 91 was a "storage capacitor common wire" (see pages 8-9 of the Office Action). However, it cannot be said that ITO 91 in Jung Mok is a "line" which is "parallel to the signal line" and which extends across a plurality of pixels as required by claim 9. Electrode 91 in Fig. 4 of Jung Mok is roughly in the shape of a square, and cannot be a "line" as required by claim 9. Moreover, the ITO 91 in Jung Mok does not extend across a plurality of pixels as required by claim 9. Accordingly, it will be appreciated that ITO electrode 91 in Jung Mok's Figs. 4-6 cannot be the storage capacitor common line recited in claim 9 for at least these two reasons.

Additionally, Jung Mok also fails to disclose or suggest a storage capacitor electrode and a storage capacitor common line *being patterned in different steps so as to have an insulation film provided partially therebetween* as required by claim 9. In Jung Mok, line 81b is both the storage capacitor electrode and the line therefore; and thus the two are formed at the same time which is the opposite of what claim 9 requires.

Furthermore, claim 9 also requires that a "storage capacitance is provided between the pixel electrode and the storage capacitor electrode." It is apparent from Fig. 5 of Jung Mok that storage capacitance is provided between transparent electrode 91 and pixel electrode 93. Thus, if the Examiner contends that the ITO electrode 91 is the line as in the last Office Action (which would be incorrect for the reasons discussed above), then this capacitance would be between the

pixel electrode and the line (not between the pixel electrode and the storage capacitor electrode as required by claim 9). Thus, even if the Examiner were to incorrect contend that in Figs. 4-6 of Jung Mok ITO 91 was a "storage capacitor common line", the invention of claim 9 still would not be met.

Claim 12 requires "a storage capacitor common line disposed at least partially parallel to the signal line so as to be electrically connected to the storage capacitor electrode, the storage capacitor common line extending across a plurality of pixels." Jung Mok fails to disclose or suggest these features of claim 12.

Claim 14 requires "a storage capacitor common line disposed at least partially parallel to the signal line so as to be electrically connected to the storage capacitor electrode, the storage capacitor common line extending across a plurality of pixels. Jung Mok fails to disclose or suggest these features of claim 14.

Claim 35 requires "a storage capacitor common line disposed at least partially parallel to the signal line so as to be electrically connected to the storage capacitor electrode, the storage capacitor common line extending across a plurality of pixels." Jung Mok fails to disclose or suggest these features of claim 35. Citation to other art cannot cure the aforesaid flaws in Jung Mok.

Claim 42 requires "a storage capacitor common line disposed parallel to the signal line so as to be connected to the storage capacitor electrode, the storage capacitor common line extending across a plurality of pixels." Jung Mok fails to disclose or suggest these features of claim 42.

It is thus requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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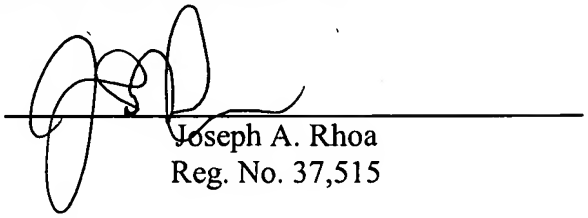
By: 

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